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DESIGN FOR DIGITAL ECG ACQUISITION SYSTEM

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Abstract: **A new power-efficient electrocardiogram acquisition system that uses a fully digital architecture to reduce the power consumption and chip area. The proposed architecture is compatible with digital CMOS technology and Multiply-Accumulator Unit (MAC), Active Electrode and Offset Cancellation are used. The circuit is implemented in 0.18-um CMOS process. This paper proposes a Finite Impulse Response (FIR) filter based on MAC unit to suppress the Power Line Interference (PLI) noise. The current work compares various MAC units on Power, Performance and Area (PPA) benchmarks. It is shown that Booth-Wallace Carry Look Ahead Adder (CLA) based on MAC is optimized for both time and power. The simulation results show that the front end circuit consumes 111mW of power.**

Keywords: ECG, CMOS, MAC Unit, Active electrode, Offset cancellation, PLI

1.INTRODUCTION

Biomedical signal processing is widely used to medically diagnose various parts of the body where ECG signal analysis is the most widely used technique for getting information on cardiac health and pathology. Through enabling continuous remote cardiac monitoring one can improve the quality of care and achieve enhanced patient autonomy and mobility for older patients. The ECG signal gives a composite snapshot of the electrical and mechanical performance of heart vs. time from several different projections or directions (different electrodes are placed on different parts of the body).

ECG signal works by detecting and amplifying the tiny electrical changes on skin caused by heart muscle "depolarization" during each heart beat. ECG signal of a normal heart beat consists of a three parts P wave, QRS complex and T wave as shown in figure 1. However, the ECG signals get distorted due to various noise sources and the extraction of information gets negatively influenced and maybe interpreted wrongly. Proper acquisition of weak signals in diverse noisy environment is one of the biggest challenges while developing an ECG filter.

Several techniques have been proposed in literature to tackle the problem of energy-efficiency in wearable ECG sensors and monitors. However, most of them focus on the ECG compression using compressed sensing signal acquisition to reduce the airtime over energy-hungry wireless links. This paper pivots around the fact that the ECG signal de-noising filter for proper interpretation of the cardiac information should be high speed and energy efficient in addition to the embedded compressed sensing which will further improve the battery life and give a better performance.

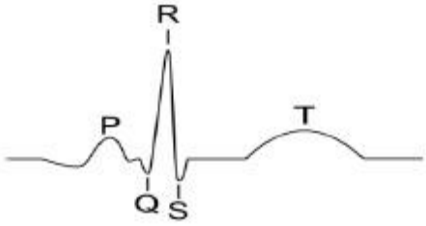

Fig.1. ECG Signal

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By using CMOS technology, the supply voltage is been reduced. Although the technology scaling leads to low power consumption and higher performance in digital circuits removal of the power line interference, base line wander and high frequency noise has been illustrated, by applying digital Infinite Impulse Response (IIR) filter on the raw ECG signal. The MAC unit design is significant for FIR filter design because it is used at every tap-summer stage and forms the core of the filter. Thus, if we are able to make a high-speed MAC unit, an efficient FIR filter can be autonomically designed which is high speed and expends less power.

II PROPOSED DESIGN FOR ECG ACQUSITION

The proposed system consists of a Multiply-Accumulator Unit, Active Electrode and Offset Cancellation shown in Figure.2. In this architecture, Voltage to Time Converter (VTC) is removed, and the impact of the Multiply-Accumulator Unit (MAC) is used instead of Voltage to Time Converter (VTC). Christo Ananth et al. [4] discussed about an eye blinking sensor. Nowadays heart attack patients are increasing day by day."Though it is tough to save the heart attack patients, we can increase the statistics of saving the life of patients & the life of others whom they are responsible for. The main design of this project is to track the heart attack of patients who are suffering from any attacks during driving and send them a medical need & thereby to stop the vehicle to ensure that the persons along them are safe from accident. Here, an eye blinking sensor is used to sense the blinking of the eye. spO2 sensor checks the pulse rate of the patient. Both are connected to micro controller.If eye blinking gets stopped then the signal is sent to the controller to make an alarm through the buffer. If spO2 sensor senses a variation in pulse or low oxygen content in blood, it may results in heart failure and therefore the controller stops the motor of the vehicle. In the following text, each of the blocks of the proposed architecture is explained.

A. Multiply-Accumulator Unit

MAC stands for Multiply-Accumulator Unit which suggests that there is a multiplication operation at every clock edge and the result in the Accumulator register is updated in the next clock edge as shown in figure 5. The figure depicts that Multiplier (A) and Multiplicand (B) of 4 bits each have to be kept stable for a specific time before and after the clock edge which is the setup and hold time of the system. The proposed system of a MAC is shown in figure.2.

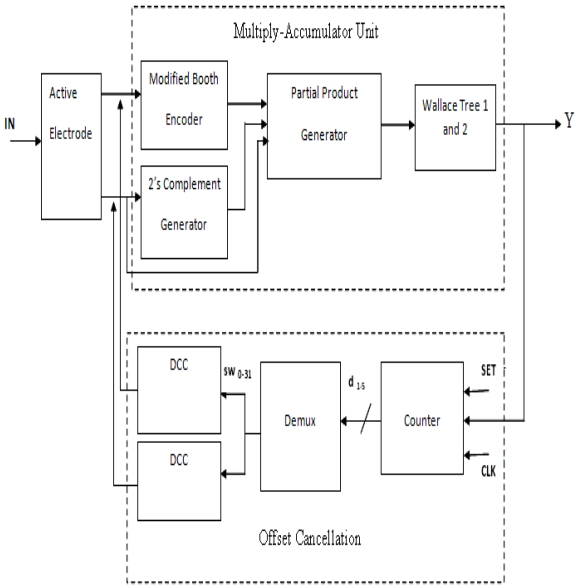

Figure.2 The Proposed Block Diagram

To design a high speed multiplier in MAC unit there can be 3 approaches:

- Reduction in the number of partial products.
- Acceleration in the formation of partial products.
- Acceleration in the addition of the partial products.

The basic architecture of a MAC is shown in figure 3. The inputs (Multiplier and Multiplicand) are of 16 bits each. The output is 32 bits after the Wallace Tree Reduction stage. This output is then given as the input to the final stage adder which generates a 33 bit result. The multiplier in the figure 4 limits the speed of the MAC unit.

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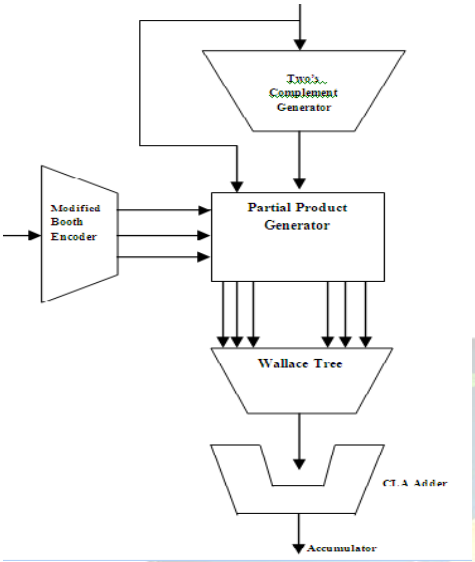

Figure.3 MAC Architecture

To design a high speed multiplier in MAC unit there can be 3 approaches such as Reduction in the number of partial products, Acceleration in the formation of partial products and Acceleration in the addition of the partial products. The proposed MAC takes into consideration all the 3 ways to increase the performance and at the same time, maintain low power. The number of partial products are reduced to half by using Radix-4 Modified Booth Algorithm in comparison to Array and Vedic multiplier. Acceleration in the reduction of partial products is done using Wallace Tree Reduction method. The final stage of MAC is addition which is done by using Wallace Tree.

B. Modified Booth Encoder

The Multiplier in the MAC unit can be built using Array Multipliers which use simple hardware but the time required is more because the number of partial products equals the number of bits of the multiplier. Using Radix-4 modified Booth's multiplier, the number of partial products are reduced to 'n/2'if we are multiplying two 'n'bits numbers, if 'n'is even number, or '(n+1)/2', if 'n'is an odd number. By reducing the number of partial products, we can effectively speed up the multiplier by a factor roughly equal to 2.

C. Partial Product Generator

A product formed by multiplying the multiplicand by one digit of the multiplier when the multiplier has more than one digit. Partial products are used as intermediate steps in calculating larger products. This reduction procedure is repeated in each successive stage until only two rows remain. Thus, Wallace tree is used to produce two rows of partial products that can be added in the last stage. Figure.2 shows the algorithm to reduce 8 partial products to 2 rows in the final stage.

D. Wallace Tree

Wallace tree reduction is used to arrange the partial products in a tree structure to reduce the number of computations by the use of full adders and half adders. However, in the reduction phase half adders do not reduce the number of partial product bits. Full adders are used in each column where there are three bits whereas half adders are used in each column where there are only two bits. Any single bit in a column is passed to the next stage in the same column without processing. The final stage of MAC is addition which is done by using Wallace Tree.

E. Active Electrode

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An active electrode is an electrode, in which some active elements are used to reduce the power line interference. Figure.3 shows two different two-wired active electrodes for comparison.

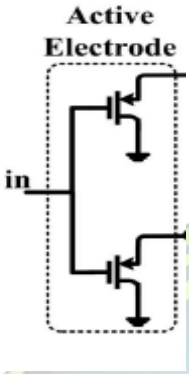

Figure.4 Active Electrode

However, the offset and the output resistance are worse. Since, in ECG applications, the most important limiting factor is the input noise of the system, we have used the active electrode with a single MOS transistor.

F. OFFSET CANCELLATION

The block diagram of the proposed offset cancellation technique is shown in Figure.2. It contains two 16-bit DCCs, 5-bit counter, and 5–32 demultiplexer (Demux). Since the offset voltage changes very slowly, the frequency of the clock signal used for the counter (Clk) is ~10 times less than the clock of the rest of the circuit.

Synchronous counters are capable of counting "Up" or counting "Down", but their is another more "Universal" type of counter that can count in both directions either Up or Down depending on the state of their input control pin and these are known as Bidirectional Counters**.** Bidirectional Counters are capable of counting in either direction through any given count sequence and they can be reversed at any point within their count sequence by using an additional control input as shown below. The DOWN (UP) signal will be set by the control logic block. The output of the counter changes accordingly and is applied to the Demux, which controls the DCC. The DCC generates a current proportional to its digital input and decreases/increases the input voltage.

G. DCC

In the fully digital ECG front-end architecture of Figure.2 two DCC blocks are used. These blocks are in charge of generating a current that depends on the 32-bit digital number (SW0 to SW31) at the output of the Demux. The DCC circuit is shown in Figure.4, in which the lower circuit generates the gate voltages required for the reference current generator in the upper circuit.

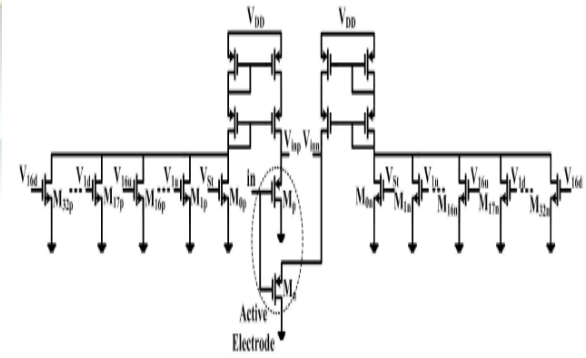

Figure.5 DCC

To better understand the behavior of the DCC, assume that the offset at the input increases

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(decreases) leading to a rise (fall) in *V*inp and *V*inn. MAC is generated by the counter and Demux. Consequently, one of the current controlling transistors (*M*1*p* to *M*32*p* for the DCC*p* and *M*1*n* to *M*32*n* for the DCC*n*) are turned ON and *V*inp and *V*inn are reduced. This procedure is repeated until the operation of the MAC blocks performed.

III SIMULATION RESULTS

The proposed architecture is implemented in 0.18-um CMOS technology. A high-performance MAC Unit is essential to design a linear FIR filter. In this section, we present the comparison of different multiplier types such as Booth-Wallace, Vedic and Array Multipliers along with Wallace Tree, RCA and CLA adders for the final stage addition in the accumulator. Table II shows the comparative analysis of the various implemented designs according to power, performance and area benchmarks. Performance is measured in terms of Critical Path Timing which is the time taken for the 1^{st} multiplier bit to multiply and store the result in the last Accumulator bit. The power comparison includes the sum of static and dynamic power calculated using the maximum transition bits. Overall, any implementation which includes the CLA adder is superior in performance than the Wallace Tree adder by approximately 18.6% because the former adder does not wait for the carry to be propagated from the previous stage.

By contrast, the RCA is the slowest adder which shows 25% average degradation in perfor- mance as compared to CLA. Although the Vedic multiplier uses a simplified algorithm for high-speed multiplication, it consumes largest area and power, out of all implemented designs. It is a well-known fact that timing and area are conflicting constraints which can be clearly seen from the results. Booth-Wallace MAC occupies less area and is one of the slowest MAC units with high power expenditure. For low power and not so timing critical applications, Array Multiplier can be used. It can also be inferred that Booth- Wallace-CLA MAC is the fastest MAC unit with 6.2% boost in performance and requires 12.1% less power than Vedic-CLA MAC.

Select Line (Encoding)	Partial Products (Operation)
000	Add 0
001	Add Multiplicand
010	Add Multiplicand
011	Add 2*Multiplicand
100	Subtract 2*Multiplicand
101	Subtract Multiplicand
110	Subtract Multiplicand
111	Subtract 0

Table I: Truth table for Booth Algorithm

The Multiplier in the MAC unit can be built using Array Multipliers which use simple hardware but the time required is more because the number of partial products equals the number of bits of the multiplier. Vedic Multiplier can also be used which uses the Urdhva-triyagbhyam Sutra[8] which is a simplistic algorithm but

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requires more hardware thus, more area. Using Radix-4 modified Booth's multiplier, the number of partial products are reduced to 'n/2' if we are multiplying two 'n' bits numbers, if 'n' is even number, or '(n+1)/2', if 'n' is an odd number. By reducing the number of partial products, we can effectively speed up the multiplier by a factor roughly equal to 2. The Booth Encoding scheme for Radix-4 Algorithm is shown in Table I.

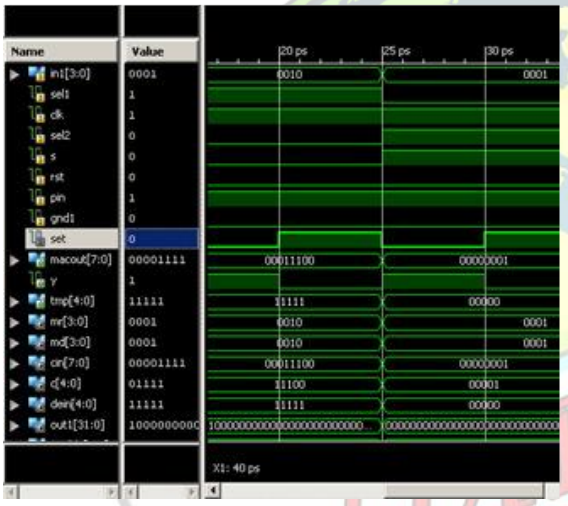

Figure 6. Simulation Result

The figure 6 shows the details of the simulation process. By setting the input value of active electrode (in1). For the MAC, input based on active electrode .such that multiplicand and multiplier values are same , which are multiply by partial product generator. The partial product generator outputs are added in Wallace tree and the MAC_out are received. The MAC outputs are enter into counterpart based on set the input value want to up / down counter. Counter output is going to demux as input and thus demux proceed the counter output to increment to 32 bits. Such that 32 bits are split into 2 block of DCC. Finally, DCC output which predict the ECG signal digital form,. if any one of y1 or y2 output is high the active electrode enable to 0 and then the ECG signal measured. The ECG signal is recovered from the noise and shown in the figure 7.

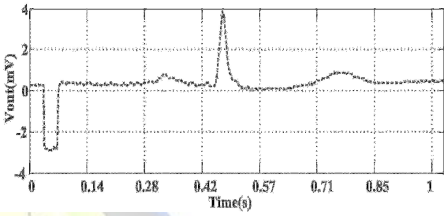

Figure 7. Recovered Signal

IV CONCULSION

Low-power and high speed filtering is required for wearable real-time monitoring of the ECG signal. To design the filter, low-power and high performance MAC unit is essential which has been discussed in this paper. The performance of the developed MAC has been analyzed and compared with other implemented MAC Units on power, timing and area benchmarks. Hence, Booth-Wallace is the preferred MAC to use in portable ECG processing applications. The FIR filter designed uses Time Division Multiplexed MAC and thus, the area of the processing unit is also minimized Thus, this high speed-low power-high density filter design can be used in portable or wearable ECG monitors.

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