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HIGH PERFORMANCE AREA EFFICIENT FIR FILTER DESIGN USING PIPELINE ADDER

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ABSTRACT:

Transpose form finite impulse response filters are inherently pipelined and support Multiple constant multiplications (MCM) technique. To modifies the FIR filter architecture and used reconfigurable applications to get a area efficient and high speed. The proposed Structure used has vedic multiplier technique block implementation of direct structure has less Area Delay Product (ADP) and Energy Per Sample (EPS) then the existing block implementation of direct form structure for medium or large filter. The basic multiplier can be used existing structure then the time delay occur to over come this using Vedic multiplier to implement high speed and get high frequency value. Then the pipeline process, compressor technique and carry save adder can be used to implementing and adding the partial products constructed the FIR (finite impulse response) without any bit error rate and increasing high speed of the performance.

I . INTRODUCTION

FINITE-IMPULSE response (FIR) digital filter is widely used in several digital signal processing applications, such as speech

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processing, loud speaker equalization, echo cancellation, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR) and soon . Many of these applications require FIR filters of large order to meet the stringent frequency specification.Very often these filters need to support high sampling rate. The MCM method on the other hand reduces the number of additions required for the realization of multiplications by common sub expression sharing, when a given input is multiplied with a set of constants. The MCM scheme is more effective, when a common operand is multiplied with more number of constants. Therefore, the MCM scheme is suitable for the implementation of large order FIR filters with fixed coefficients. But, MCM blocks can be formed only in the transpose form configuration of FIR filters Another hardware-efficient implementation of programmable FIR filters with CSD coefficients has been presented in . A 32-tap linear-phase filter, with two nonzero CSDs in each tap, is implemented. Additional nonzero CSDs can be allocated to specific filter taps, making it a reconfigurable FIR filter architecture.Techniques that yield an FIR filter with the minimum total number of CSD for a given frequency response specification can be found in and we have developed a software program based on fir filter. The filter implemented with this architecture can be easily configured as a matched filter, a pulse-shaping filter, or other filters. Furthermore, the proposed FIR architecture also has scalability, modularity.

II. COMPUTATIONAL ANALYSIS AND MATHEMATICAL FORMULATION OF BLOCK TRANSPOSE FORM FIR FILTER

The data-flow graphs (DFG-1 and DFG-2) of transpose form FIR filter for filter length $N = 6$, as DFG of transpose form structure for $N = 6$. DFG-1 for output $y(n)$. DFG-2 for output $y(n-1)$. DFT of multipliers of DFG shown in corresponding to output $y(n)$. DFT of multipliers of DFG shown in corresponding to output $y(n-1)$. Arrow: accumulation path of the products. a block of two successive outputs $\{y(n), y(n-1)\}$ that are derived from . The product values and their accumulation paths in DFG-1 and DFG-2 of are shown in dataflow tables (DFT-1 and DFT-2) of The arrows inDFT-1 and DFT-2 of represent the accumulation path of the products.

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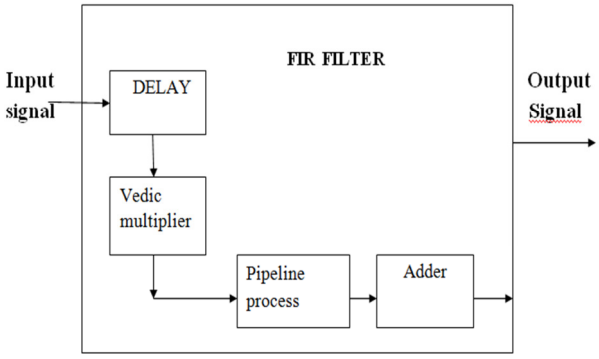
PROPOSED METHOD:

A fast method for multiplication based on ancient Indian Vedic mathematics is proposed in this paper. Among the various methods of multiplications in Vedic mathematics, Urdhva tiryakbhyam is discussed in detail. Urdhva tiryakbhyam is a general multiplication formula applicable to all cases of multiplication. This algorithm is applied to digital arithmetic and multiplier architecture is formulated. This is a highly modular design in which smaller blocks can be used to build higher blocks. The coding is done in VHDL (very high speed integrated circuits hardware description language) and synthesis is done using Xilinx ISE series. The combinational delay obtained after synthesis is compared with the performance of the modified Booth Wallace multiplier which is a fast multiplier. This Vedic multiplier can bring about great improvement in DSP performance.

BLOCK DIAGRAM:



FIR FILTER:

In signal processing, a finite impulse response (**FIR**)**filter** is a **filter** whose impulse response (or response to any finite length input) is of finite duration, because it settles to zero in finite time.

DELAY:

The act of postponing, hindering, or causing something to occur more slowly than normal **the** state of being delayed.

VEDIC MULTIPLIER:

Some time ago (this past summer, to be exact) I created my first instructable. A fun little trick, really, about how to quickly extract the cube roots of large integers mentally. Included in the comments section of this instructable was a very useful

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comment from mahi16 which suggested I incorporate Vedic Mathematics methods into my technique.

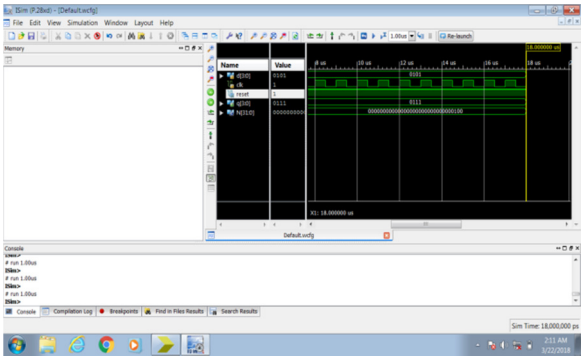
PIPELINE PROCESS:

In computing, is a set of data path processing elements connected in series, where the output of one element is the input of the next one. The elements of the pipeline are often executed in parallel or in time-sliced fashion; in that case, some amount of buffer storage is often inserted between elements. Computer-related ...intrigued by the clever strategies employed in the ancient Indian system. I got a book on it this year for Christmas and am researching the different techniques and methodologies presented in it.

ADDER:

A adder is a digital thatis digital circuit performs addition of numbers. In many computers and other kinds of processor that adder are used in the arithmetic logic units or ALU. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement opera.

OUTPUT:



CONCLUSION:

To reconfiguring the fir filter architecture that can be used to get a high area efficient and increase performance of the speed using the proposed system vedic multiplier for speedy operations not only for mental calculations but also hardware implementations. Redusing the time delay occurance and get a high speed levels of frequency val**ue.**

REFERENCES:

[1] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms and Applications*. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.

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[2] T. Hentschel and G. Fettweis, "Software radio receivers," in *CDMA Techniques for Third Generation Mobile Systems*. Dordrecht, The Netherlands: Kluwer, 1999, pp. 257–283.

[3] E. Mirchandani, R. L. Zinser, Jr., and J. B. Evans, "A new adaptive noise cancellation scheme in the presence of crosstalk [speech signals]," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 10, pp. 681–694, Oct. 1995.

[4] D. Xu and J. Chiu, "Design of a high-order FIR digital filtering and variable gain ranging seismic data acquisition system," in *Proc. IEEE Southeastcon*, Apr. 1993, p. 1–6.

[5] J. Mitola, *Software Radio Architecture: Object-Oriented Approaches to Wireless Systems Engineering*. New York, NY, USA: Wiley, 2000.