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A TLC for Optimizing Power in Embedded Processor

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Abstract: Segmentation memory technique is a system of addressing computer memory, which may be physical or virtual and may be operating in real or protected mode. Generally load/store queue is using for cache memory accesses the ETA can be match data values and address quickly. In ETA consist of LSQ tag array and LSQ TLB, here tag array will be segment the memory that time power will increase. The power and area can be reduces by memory segmentation technique. The cache design is more effective in area and power reduction. The proposed technique can be configured under two operation modes to exploit the tradeoffs between energy efficiency and performance. It is shown that our technique is very effective in reducing the number of ways accessed during cache accesses Energy consumption can be reduced greatly because at most only one data array corresponding to the matched tag, if any, is accessed. Due to the increase in access cycles, phased caches are usually applied in the lower level memory, such as L2 caches, whose performance is relatively less critical. Thus, only one way needed to be accessed during the cache access stage if the prediction is correct, thereby reducing the energy consumption significantly.

Keywords: TLC, ETA, TLB

I. INTRODUCTION

A cache is a component that transparently stores data so that future requests for that data can be served faster. The data that is stored within a Cache might be values that have been computed earlier or duplicates of original values that are stored elsewhere. If requested data is contained in the cache (cache hit), this request can be served by simply reading the cache, which is comparatively faster. Otherwise (caches miss), the data has to be recomputed or fetched from its original storage location, which is comparatively slower. Hence, the greater the number of requests that can be served from the cache, the faster the overall system performance becomes. Here Miss/Hit occurs means data cache is used. Small amount of fast memory Sits between normal main memory and CPU May be located on CPU chip or module.

In data's are continuously stored like RAM. In L2 data's are store just like Hard disk. Cache memory is fast and it is expensive. It is categorized in levels that describe its closeness and accessibility to the microprocessor. Level 1 (L1) cache, which is extremely quick but relatively small, is located close to the processor and it is used to access the easy and fast. Level 2 (L2) cache is located half-way between the process and the system bus; it is fairly high-speed and medium-sized. The modified load store queue "caches" all previously accessed data values going beyond existing store-to-load forwarding techniques. Both load and store data are placed in the LSQ and are retained there after a corresponding memory access instruction has been committed. A memory management unit (MMU) that fetches page table entries from main memory has a specialized cache, used for recording the results of virtual address to physical address translations. This specialized cache is called a translation look aside buffer (TLB).Dividing the cache into separate tag and data arrays reduces the access time of the cache. The tag array typically contains many fewer bits than the data array can therefore be accessed more quickly than either the data array or a single combined tag/data array.

II. EXISTING METHOD

2.1 LSQ TAGARRAY AND LSQ TLB

To ignore the data conflict with the L1 data cache, the LSQ tag arrays and LSQ TLB are implemented as a copy of the tag arrays and TLB of the L1 data cache, respectively. There are two types of operations in the LSQ tag arrays andLSQ TLB: lookup and update. Each time a recollection address the LSQ, the LSQ tag arrays and LSQ TLB will be searched for the premature destination way. In case of a hit, the early destination way will be available; If not, the instruction will cause either an early tag miss (if the access to the LSQ tag arrays encounters a miss) or an early TLB miss (if the address is not in the LSQ TLB). For inform operations, the contents of LSQ tag arrays and LSQ TLB is efficient with the tag arrays and TLB of the L1 cache, so that they are identical to avoid cache consistency harms. The update logic of LSQ tag arrays and LSQ TLB is the

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equivalent as that of the tag arrays and TLB of the L1 cache.The LSQ tag arrays, where only one way is shown as the other ways are the same. Consider that generally at most *N* instructions can enter the LSQ while the L1 data cache allows *M* substitute to occur at the same time. Consequently, there force is at most *N* lookup operations and *M* update operations occurring at the LSQ tag arrays and LSQ TLB at the same time. In order to perform these operations simultaneously, the LSQ tag arrays and LSQ TLB have *N* read ports and *M* write ports. Write/read conflicts occur when the lookup and update operations purpose the same location the LSQ tag arrays at the same time. To address this issue, we disable the lookup operation if an update operation is currently performed. This is achieved by the control signal lookup-disable, which is a generated by the way enable signal from the cache controller for cache replacements. Regard as a two-way set-associative cache for example. Assume that there is a replacement occurring at the way 1 of the L1 data cache. While a result, the way enabling signal is position to "1" and then sent to the NAND gates in the way 1 of the LSQ tag arrays. If the write decoder outputs a "0," i.e., no update operation on this entry of the tag array, the lookup-disable signal will be set to "1" and the activate circuit will not block the lookup operation on this entry. Otherwise the lookup-disable signal will be "0," and the activate circuit will block possible lookup operations to avoid write/read conflicts. The lookup operation, if any in this case, is considered as a miss. This miss might cause some performance degradations if it turns out to be a cache hit in the cache access stage. We observed from simulations less than 0.01% of the total LSQ accesses experienced this issue. Note that if the way enabling signal is "0," i.e., no update operation, the lookup operation will not be affected. This scheme is also used in the LSQ TLB. Since the activating circuit introduces no performance consequence, the enabling circuits increase the critical path of the LSQ tag arrays and LSQ TLB by the delay of an NAND gate. This delay is slight as compared with the critical path of the L1 data cache.In the below block diagram index data is given as input to the information buffer and its values are passed to multiplexer and TLB.Then, TLB split into two tag arrays (one for odd priority and another one for even priority) with help of comparator. When hit/miss occurs in way decoder, it can be controlled by cache controller. If hit/miss '0', the value will go to the first data array otherwise it will go to the second data array. The communication protocol is used for transferring data's and TLB is used for data address and RS232.The way decoder is used for the fast access and early destination way.

III. Proposed Technique

3.1 INBUILT MEMORY SEGMENTATION

Memory segmentation is the division of a computer's primary memory into segments or sections. In a computer system using segmentation, a reference to a memory location includes a value that identifies a segment and an offset within that segment. Segments or sections are also used in object files of compiled programs when they are linked together into a program image and when the image is loaded into memory. The Intel 8086 processor generation was designed to address as much as 1MB of memory but was hampered by the limits of flat address space. Rather than redesign the entire memory system, Intel modified it to achieve the greater capacity through a two-part, segment.Memory management, the memory controller needs to know where in physical memory are the start and the end of each segment. When segments are replaced, a single segment can only be replaced by a segment of the same size, or by a smaller segment. After a time this results in a ``memory fragmentation", with many small segments residing in memory, having small gaps between them.

Inbuilt memory segmentation is used to reduce the power, area and also access the data in fast time. It increases the performance also. All the components consider as inbuilt/fixed such as multiplexer, tag array and data memory. Here TLB address is same as virtual address and Index data is given as input of information buffer. Consider MSB bit for initial checking and select lines s1, s2 and s3 after only checking the LSB bit. If memory segmentation and TLB address equal means goes to another bit otherwise hit/miss will.

IV. Performance Analyses

4.1 Power Analysis

The power of cache memory using tlc, memory

Various technique	Power (W)
TAG LESS CACHE TECHNIQUE	0.322
MEMORY SEGMENTATION	0.565
LSQ TLB AND LSQ TAG ARRAY	0.944

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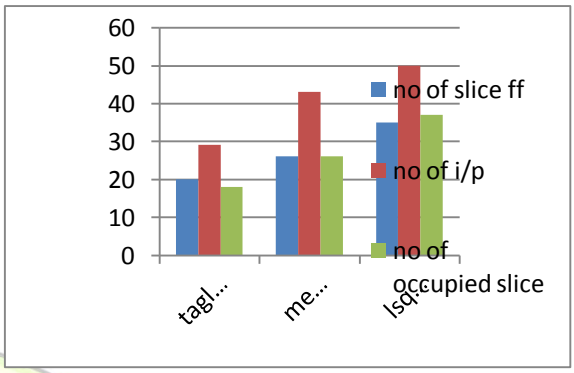
Various technique	Number of slice flip flops	Number of input LUTS	Number of occupied slices
Tag Less Cache Technique	20	29	18
Memory Segmentation	26	43	26
LSQ TLB And LSQ Tag Array	35	50	37



segmentation technique, LSQ TLB and LSQ tag array are compared and tabulated in table 5.1. It consumes less power and area. It shows a bar chart with power in y-axis and various techniques in x- axis. From the figure 4.1analysis the power using various technique. The tlc possess lower power compared to the memory segmentation, LSQ cache achitecture. The early tag access uses the advantage of reducing the critical path in the circuit and operates faster with lower power and area. The area of cache memory using memory segmentation technique, LSQ TLB and LSQ tag array, information buffer and tag array are compared and tabulated in table 4.2 It consumes less area and increase the performance. It shows a bar chart with area in y-axis and various logic utilization in x- axis. From the figure 4.2 using memory segmentation technique is reduced the area compare with various technique

TABLE4.1
AREA ANALYSIS

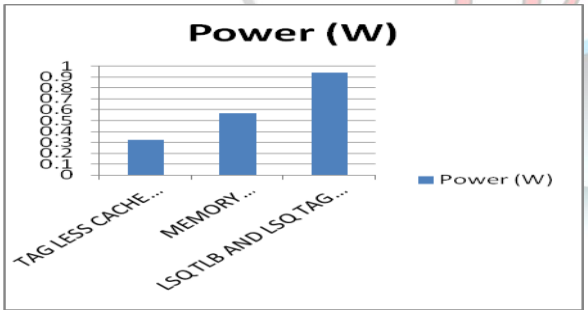


Table 4.2
AREA ANALYSIS

V. SIMULATION RESULTS

The proposed technique memory segmentation compare with various technique using VHDL in Xilinx software. To improve the energy efficiency reduces the area, power and checking the address with data quickly. In figure 5.3, Information buffer to hold the early destination way until the corresponding load/store instruction is issued to the L1 data cache. In each entry, the tag miss and TLB miss bits ("1" for hit and "0" for miss) indicate the status of early tag and early TLB accesses, respectively. In figure 5.4, tag array is used to reduce the data collision and usd to select the address as temporary. To ignore the data contention with the L1 data cache, the LSQ tag arrays and LSQ TLB are implemented as a copy of the tag arrays and tlb.

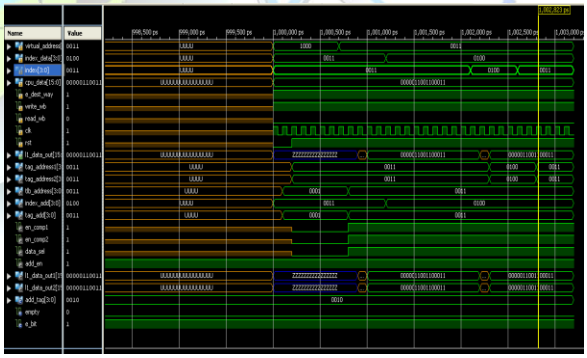


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Figure 5.1 LSQ TLB and LSQ TAG ARRAY

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.193	1	...	...
Logic	0.001	28	4896	1
Signals	0.004	58	...	...
IOs	0.682	42	108	39
Leakage	0.065			
Total	0.944			

Figure 5.2 Power of LSQ

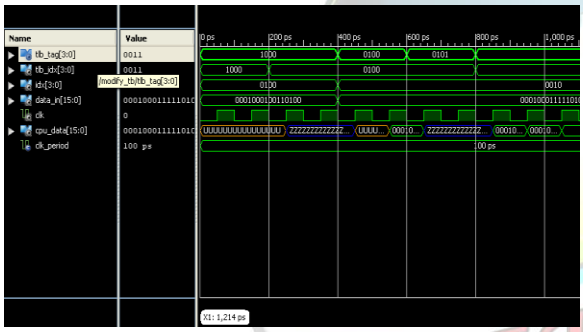

Figure 5.5 Tagless Cache Techniques

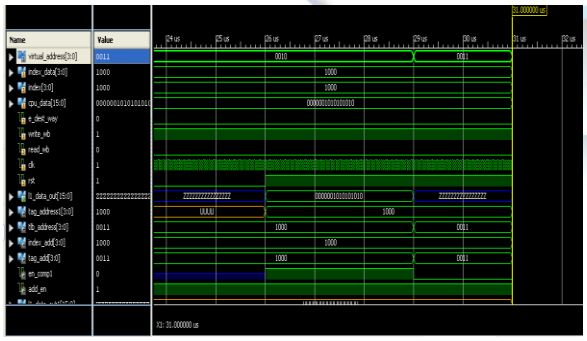

Figure 5.3 Memory segmentation techniques

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.221	1	...	...
Logic	0.000	43	4896	1
Signals	0.002	71	...	...
IOs	0.284	41	108	38
Leakage	0.059			
Total	0.565			

Figure 5.4 Power of Memory Segmentation

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.215	1	...	...
Logic	0.000	29	4896	1
Signals	0.001	59	...	...
IOs	0.052	45	158	28
Leakage	0.055			
Total	0.322			

Figure 5.6 Power of Tag less Cache Techniques

VI. CONCLUSION

A new energy-efficient cache design technique for low-power embedded processors. The memory segmentation technique predicts the destination way of a memory instruction at the early LSQ stage. Thus, only one way needed to be accessed during the cache access stage if the prediction is correct, thereby reducing the energy consumption significantly. By applying the idea of phased access to the memory instructions whose early destination ways cannot be determined at the LSQ stage, the energy consumption can be further reduced with negligible performance degradation. Simulation results demonstrated the effectiveness of the proposed technique as well as the performance impact and design overhead. While our technique was demonstrated by a L1 data cache design and to deal with multithreaded workloads. It save memory if segments are very small and should not be combined into one page compare to the previous technique power of memory segmentation was reduced to 0.565W rather than 0.944W.It is used to access fast time and also reduces power and area.

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Memory can be segment and check MSB bit, saves time reduces the data collision.

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