



# An Optimised Diminished One Modulo $2^n+1$ Low Power Static And Dynamic Adder Using Circular Carry Selection

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**Abstract:** The diminished-one modulo  $2^n+1$  addition is an important arithmetic operation for a high-performance residue number system. In this paper, we propose a new circular-carry-selection (CCS) technique for modulo  $2^n+1$  addition in the diminished-one number domain. The architecture design of CCS is technique for modulo  $2^n+1$  addition in the diminished-one number domain. The architecture design of CCS modular adder is simple and regular for various bit-width inputs. Low power static and dynamic adder technique is used for actual VLSI implementation; the proposed modular adder can demonstrate its superiority of savings up to 39.5% in Area Time and 46.3% in Timex Power performances over those of the previous existing solutions under 180-nm CMOS technology. Finally, the chip area and the clock rate of CCS diminished-one modulo  $2^{16}+1$  adder are 26746 $\mu$ m<sup>2</sup> and 476MHz, respectively.

**Keywords:** circular carry selection (CCS) modulo  $2^n+1$  adder, residue number system (RNS), VLSI design.

