



Analysis of Deep Submicron Device parameters Using T-Sizing

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Abstract: The variations that are seen in the semiconductor fabrication process causing changes in threshold voltage, oxide thickness, channel length, interconnect wire width, thickness, etc. is referred as process variation. Optimization of Complementary Metal Oxide Semiconductor (CMOS) circuit is to discover the variation in physical parameters which affects the circuit performance such delay, power dissipation. Circuit delay is particularly sensitive to process variations because it is dependent on a number of other variation-sensitive parameters. Variation in delay also changes the dynamic power dissipation. This effect is the reasons for considering process variation effect in estimating the power. In the proposed work, by using Transistor sizing (T- sizing) we analyze the parameter variations, such as voltage, current, frequency and temperature. To predict electrical behavior of the device we have analyzed the CMOS performance using circuit simulator and proved that process variations will affect electrical characteristics of a device.

Keywords: CMOS, Optimization, Power dissipation, T-sizing

