International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 3, November 2014

A Robust Design of Highly Efficient Dynamic Comparator Using Wave Pipelining

G.S.Sankari[1], S.Belwin Joel[2], S.Siraj Fathima[3]

Assistant professor, Dept. of ECE, M.A.M College of Engineering & Technology, Trichy, Tamilnadu[1].
Assistant professor, Dept. of ECE, James College of Engineering and Technology, Nagercoil, Tamilnadu[2].
Assistant professor, Dept. of ECE, M.A.M College of Engineering & Technology, Trichy, Tamilnadu[3].

Abstract: A new CMOS dynamic comparator using dual input single output differential amplifier as latch stage suitable for high speed analog-to-digital converters with high speed, low power dissipation and immune to noise than the previous reported work is proposed. As compared to the existing design layout that consists of switching flip-flops, which shows high delay time and more power consumption during operations. In order to avoid these problems there by minimizing delay time and consuming less power. Back to- back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a lower power dissipation, higher speed, less area, and it is shown to be very robust against transistor mismatch, noise immunity. Layouts of the proposed comparator have been done in Model-Sim Design Environment.

Keywords: Double-tail comparator, switch flip-flop, inverter buffer, differential amplifier**.**