International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 3, November 2014

Analysis of Deep Submicron Device parameters Using T-Sizing

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Abstract: The variations that are seen in the semiconductor fabrication process causing changes in threshold voltage, oxide thickness, channel length, interconnect wire width, thickness, etc. is referred as process variation. Optimization of Complementary Metal Oxide Semiconductor (CMOS) circuit is to discover the variation in physical parameters which affects the circuit performance such delay, power dissipation. Circuit delay is particularly sensitive to process variations because it is dependent on a number of other variation-sensitive parameters. Variation in delay also changes the dynamic power dissipation. This effect is the reasons for considering process variation effect in estimating the power. In the proposed work, by using Transistor sizing (T- sizing) we analyze the parameter variations, such as voltage, current, frequency and temperature. To predict electrical behavior of the device we have analyzed the CMOS performance using circuit simulator and proved that process variations will affect electrical characteristics of a device.

Keywords: CMOS, Optimization, Power dissipation, T-sizing

I. INTRODUCTION

The growth of the semiconductor industry is obtained from International Technology Roadmap for Semiconductors (ITRS). Moore's Law states that number of transistors in a chips doubles every year. The target of scaling is improving performance through optimization of the given design. TABLE I show the 2011–2017 Roadmap for power supply and power dissipation for CMOS circuits obtained from the ITRS 2011 [1]. As technology scales, strict limitation of the allowable maximum power is projected; from 0.52W in 2011 to 0.42W in 2017.According to the ITRS the feature size will continue to scale down at the rate of 0.7 x per generation to reach 22nm [1]. The rapid development in Very Large Scale Integration (VLSI) has continued to decrease the feature size of transistors. The transistor power and performance can be varied by changing the supply voltage, temperature, width, channel length, oxide thickness and interconnect dimension of transistor.

To enhance optimization of area, power and speed several optimization methods have been developed over the years. These optimization schemes achieve an optimal balance between power and speed. In deep submicron technology era, we are in need of a new method of optimization which can make high yield without compromising area, speed and power [2].Although VLSI circuits can be optimized in a number of ways, there exists few reasons for using transistor sizing. For enhancing power /delay ratio of VLSI circuit, T-sizing is considered to be a simple but a powerful tool.

The paper is discussed into six sections. Each section is discussed briefly in this section. Section II deals with the impact of transistor sizing in the world of optimization and also deals with the impact of delay and power dissipation in the circuit. Section III discusses the literature survey on transistor sizing. Section IV elaborates the primary effect of process scaling and also the types of scaling. It also deals with the impact of scaling on power consumption and circuit performance. Section V deals with the process variation and its effect on circuit performance. It also deals with important variations seen in devices such as channel length, doping concentration and oxide thickness. Section VI discusses about the result yielded in this paper using circuit simulator.

II. SIGNIFICANCE OF T-SIZING

Transistor sizing in a combinational gate circuit can have significant impact on circuit delay and power dissipation. If the transistors in a given gate are increased in size, then the delay of the gate decreases, however, power dissipated in the gate increases. Further, the delay of the fan-in gates increases because of increased load capacitance. Given a

delay constraint, finding an appropriate sizing of transistors that minimizes power dissipation is a computationally difficult problem. A typical approach to the problem is to compute the slack at each gate in the circuit, where the slack of a gate corresponds to how much the gate can be slowed down without affecting the critical delay of the circuit [3]. T-sizing is important for implementing high yield circuit because of the following reasons.

1. Behaviour and performance of a circuit can be analyzed with continued reduction of transistor size.
2. To ensure proper functionality of a circuit
3. To maintain sufficient noise margin.

III. Review On T-Sizing

A linear method is used to make a trade –off between power, delay and area in CMOS circuits is illustrated in the work [4]. In [5], the sizing problem is formulated as a constrained non linear optimization problem. In [6], the size of transistor is varied till the optimization is achieved. In [7], the usage of transistor grouping results in lesser execution time and increased optimization rate. In [8], the T-sizing is considered to be a search problem in large multidimensional search space. By using genetic algorithm the search problem complexity can be reduced. In [9] , dual threshold voltage assignment with transistor sizing reduced the total power consumption. The trade off between static and dynamic power consumption has been explored.

In [10], transistor sizing problem is considered as two sub problems, first is logic- path gate sizing and second is gate transistor sizing. The sizes of the individual gates are obtained using logic-path gate sizing. Gate-transistor sizing decides the best actual transistor sizes of each gate to minimize the power. In [11] ,the transistor on critical paths are sized to yield better performance and reduce delay. A set of non linear constrains are framed and are solved by the algorithm which reduces delay, power dissipation through optimizing the transistor sizes on the critical path.

IV. Technology Scaling

In 1975, Moore predicted that the number of transistors per square inch in an IC will double every 18 months is shown in Figure 1. With each new process generation, the entire lateral and some of the vertical dimensions of the transistors are scaled down to allow a higher level of integration [1]

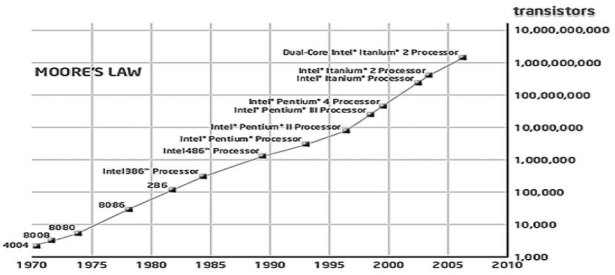

Fig 1 Moore's Law

Scaled dimensions and doping densities have an immediate impact on reducing the power dissipation, as well as increasing the circuit speed. The primary effect of process scaling is the reduction of all the capacitance, which provides a proportional decrease in the power and circuit delays [10].

In practice, there are two types of scaling strategies for MOSFET devices: constant field scaling and constant voltage scaling. In called constant field scaling, all the horizontal and vertical dimension of the transistor, as well as the power supply, is scaled down by a factor of S. In constant voltage scaling, all the dimensions of the MOSFET are reduced by a factor of S, but the power supply voltage and the terminal voltage remain unchanged [16].

TABLE I
INFLUENCE OF SCALING ON CMOS DEVICE PARAMETERS

Parameter	*Constant field scaling*	*Constant voltage scaling*
Channel length(L)	*1/S*	*1/S*
Channel width(W)	*1/S*	*1/S*
Gate oxide thickness(t_{ox})	*1/S*	*1/S*
Supply voltage (V_{DD})	*1/S*	*1*
Threshold voltage (V_{th})	*1/S*	*1*
Delay(τ)	*1/S*	*$1/S^2$*
Power dissipation(P)	*$1/S^2$*	*S*
Power delay product(PDP)	*$1/S^3$*	*1/S*
Drain current	*1/S*	*S*

A. Impact of scaling on power consumption

Power dissipation has emerged as an important design parameter in the design of microelectronic circuits, especially in portable computing and personal

communication applications [17]. Sources of power dissipation in CMOS devices are summarized by the following expression:

$$P = \frac{1}{2}.\bar{C}.V_{DD}^2.f.N + Q_{SC}.V_{DD}.f.N + I_{Leak}.V_{DD}$$

where P denotes the total power, V_{DD} is the supply voltage, and f is the frequency of operation.

The first term represents the power required to charge and discharge circuit nodes. Node capacitances are represented by C. The factor N is the switching activity, i.e., the number of gate output transitions per clock cycle. The second term in Eqn. 1 represents power dissipation during output transitions due to current flowing from the supply to ground. This current is often called short-circuit current [18], [19]. The factor Q_{SC} represents the quantity of charge carried by the short-circuit current per transition. The third term in Eqn. 1 represents static power dissipation due to leakage current I_{leak} [13]. Device source and drain diffusions from parasitic diodes with bulk regions. Reverse bias currents in these diodes dissipate power. Sub threshold transistor currents also dissipate power. In the sequel, we will refer to the three terms above as switching activity power, short-circuit power and leakage current power. Most of the optimizations described in the following sections concentrate on minimizing switching activity power at various levels of abstraction. In VLSI circuits that use well-designed logic-gates, switching activity power accounts for over 90% of the total power dissipation [8].Dynamic power and leakage current are the major sources of power consumption in CMOS circuits. Leakage related power consumption has become more significant as threshold voltage scales with technology [14]. There are several studies that deal with the impact of technology scaling in various aspects of CMOS VLSI design. Figure 2 illustrates the dynamic and leakage power consumption variation across technologies, where P_{act} is the dynamic power consumption and P_{leak} is the leakage power consumption. The estimates have only captured the influence of sub-threshold currents since they are the dominant leakage mechanism [20]. For sub-100nm technologies, temperature has a much greater impact on the leakage power consumption than the active power consumption for the same technology. In addition, the leakage power consumption increases almost exponentially [12].

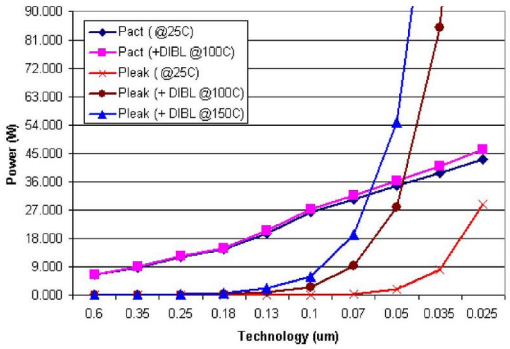

Fig 2 Active and leakage power for a constant die size

B. Impact of scaling on circuit performance

Transistor scaling is the prime factor in achieving high-performance devices. Each 30% reduction in CMOS IC technology node scaling has reduced the gate delay by 30%, reduced the parasitic capacitance by 30%, reduced energy and active power per transition by 65% and 50%, respectively and doubled the device density. Figure 3 shows CMOS performance, power density and circuit density trends, indicating a linear circuit performance as a result of technology scaling [15].

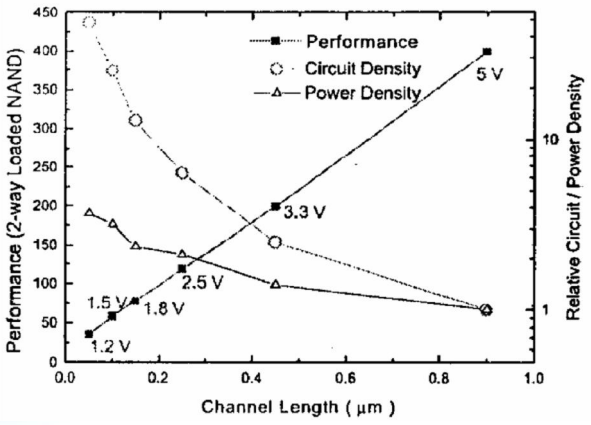

Fig 3 CMOS performance, power density and circuit density trends

V. Effect Of Process Variation On Power

The increased variation of process parameters of nanoscale devices not only results in a higher leakage but also causes a larger standard variation of leakage power [21]. In [23], twenty times difference in leakage and thirty percent variation in performance are observed. Some low leakage chips with very slow speeds and some other faster but very leaky chips have to be discarded. Therefore, both

power yield and timing yield are seriously affected by the process variation. Process variations are basically divided into inter-die and intra-die variations. Inter-die variation or global variation refers to variation from wafer to wafer, or die to die on a same wafer, while intra-die variation, or local variation, occurs across an individual die. That means that on the same chip, devices at different locations may have different process parameters. Since inter-die variation affects all the devices on a chip in the same way, it has a stronger effect on power and performance.

Channel length, doping concentration and oxide thickness are the most important variations in devices. Oxide thickness is well controlled and generally only its inter-die variation is considered. Its effect on performance and power are often lumped into the channel length variation. Channel length variations are caused by photolithography proximity effects and deviation in the optics. Threshold voltages vary due to different doping concentration and annealing effects, mobile charge in the gate oxide, and discrete dopant variations caused by the small number of dopant atoms in tiny transistors [22].

Due to the exponential relation of leakage current with process parameters, such as the effective gate length, oxide thickness and doping concentration, process variations can cause a significant increase in the leakage current. Gate leakage is most sensitive to the variation in oxide thickness (*Tox*), while the subthreshold current is extremely sensitive to the variation in effective gate length (*Leff*), oxide thickness (*Tox*) and doping concentration (*Ndop*). Twenty percent variations in effective channel length and oxide thickness can cause up to 13 and 15 times differences, respectively, in the amount of subthreshold leakage current. Gate leakage can have 8 times difference due to a 20% variation in oxide thickness. Compared with the gate leakage, the subthreshold leakage is more sensitive to parameter variations [24].

VI. Result And Discussion

To improve the modeling accuracy for sub-micron technologies, a new device modeling scheme has been proposed. This method has been demonstrated to give a better performance in submicron technology compared to other. It is also revealed that the intentional variation that is created over the physical parameters play an important role in modeling a device. The width and length of the transistor is varied step by step to find the gradual change in the output parameters. This scheme is implemented and verified in sub-micron technologies. Circuit simulator results shown in Table 2 prove that an optimized design can yield a good performance.

TABLE II

VARIATION OF V_{DD} AND PROPAGATION DELAY WITH RESPECT TO GEOMETRICAL PARAMETERS

Device geometry ratio w/l (µm)	**Output voltage (V)**	**Delay time(s)**
5/3	5	0.5
3/2	4.8	0.3
2/1	4.5	<0.1

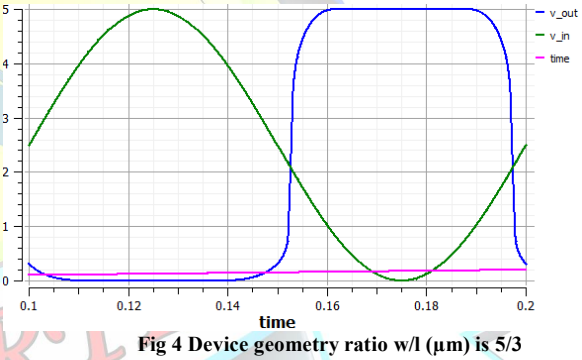

Fig 4 Device geometry ratio w/l (µm) is 5/3

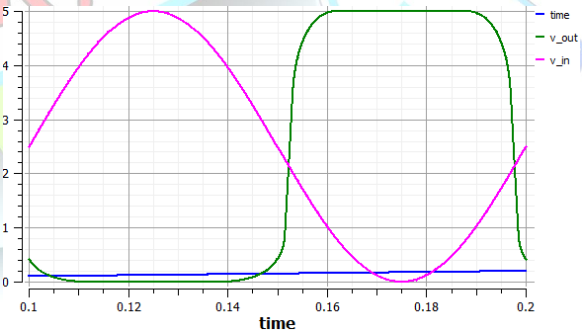

Fig 5 Device geometry ratio w/l (µm) is 3/2

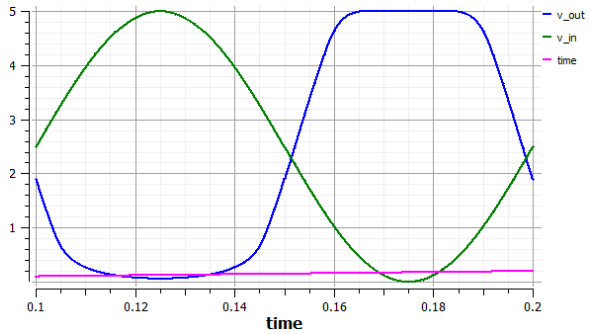

Fig 6 Device geometry ratio w/l (µm) is 2/1

VI. CONCLUSION

In summary, low power design requires a redefining of the conventional design process, where power concerns are often overridden by performance and area considerations. The need for lower power systems is being driven by many market sectors. Unfortunately designing for low power adds another dimension to the design problem. The design has been optimized for power which in turn optimizes the performance and power dissipation. The problem is further complicated by the need to optimize the design for power at all design phases. A robust design may need to consider other effects, such as process variation, which will be implemented in the future work.

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BIOGRAPHY

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