International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 1, Issue 3, November 2014

A Robust Design of Highly Efficient Dynamic Comparator Using Wave Pipelining

G.S.Sankari[1], S.Belwin Joel[2], S.Siraj Fathima[3]

Assistant professor, Dept. of ECE, M.A.M College of Engineering & Technology, Trichy, Tamilnadu[1].
Assistant professor, Dept. of ECE, James College of Engineering and Technology, Nagercoil, Tamilnadu[2].
Assistant professor, Dept. of ECE, M.A.M College of Engineering & Technology, Trichy, Tamilnadu[3].

Abstract: A new CMOS dynamic comparator using dual input single output differential amplifier as latch stage suitable for high speed analog-to-digital converters with high speed, low power dissipation and immune to noise than the previous reported work is proposed. As compared to the existing design layout that consists of switching flip-flops, which shows high delay time and more power consumption during operations. In order to avoid these problems there by minimizing delay time and consuming less power. Back to- back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a lower power dissipation, higher speed, less area, and it is shown to be very robust against transistor mismatch, noise immunity. Layouts of the proposed comparator have been done in Model-Sim Design Environment.

Keywords: Double-tail comparator, switch flip-flop, inverter buffer, differential amplifier**.**

I. INTRODUCTION

From the device mismatches such as threshold voltage, current factor $\beta(=\mu C_{ox}W/L)$ and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators.

In this paper, we present a new double-tail dual-rail dynamic comparator which shows lower input-voltage and lesser delay time than the conventional dual-rail dynamic comparators. The remaining sections of the paper are organized as follows. Section II provides the operation of the existing comparator and the performance comparisons with the previous works, section III describes the optimization of the proposed comparator and the conclusion is followed in section IV.

II. HIGH SPEED REGENARATIVE COMPARATOR

In many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. Designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed.

A. Conventional Dual-Rail Dynamic Comparator

In this system a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator.

Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the dual rail comparator is to increase _*V*fn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4 transistors but in a cross-coupled manner.

B. Operation

During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn

and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues falling, the corresponding pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which _*V*fn/fp is just a function of input transistor transconductance and input voltage difference in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (*M*c1) turns on, pulling the other node fp back to the *V*DD. Therefore by the time passing, the difference between fn and fp (*V*fn/fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

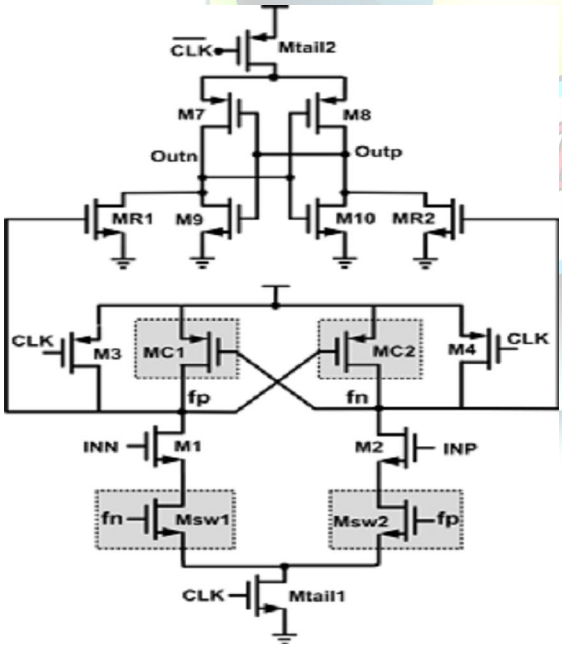

Fig. 1 Schematic diagram of the dual-rail dynamic comparator

The latch stage of this dual-rail dynamic comparator is to increase the environmental noise during the operation and the voltage becomes reduced.

C. Simulation Output

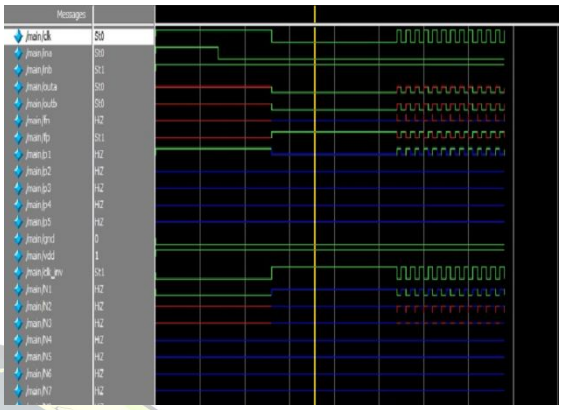

Fig 2 simulation output of dynamic comparator

The designed dynamic comparator was simulated using modelsim. In every clk pulse is given in the input of the comparator the output becomes changed respectively. The nmos and pmos transistors are used in the circuit so the operations are done respective given input. In the positive and negative edge the output become triggered.

TABLE 1
SUMMARY OF POWER OF THE COMPARATOR

Name	Power (W)	Used	Total Available	Utilization (%)
Clocks	0.010	1	---	---
Logic	0.000	1313	28800	4.6
Signals	0.000	1672	---	---
IOs	0.000	107	542	19.7
Total Quiescent Power	**0.443**			
Total Dynamic Power	**0.010**			
Total Power	**0.454**			

TABLE 2
SUMMARY OF DELAY OF THE COMPARATOR

Name	Power (W)	Voltage	Range	Icc (A)	Iccq (A)
Vccint	0.296	1.00	0.95 to 1.05	0.010	0.285
Vccaux	0.155	2.5		0.000	0.062
Vcco25	0.003	2.5		0.000	0.001

III. PROPOSED COMPARATOR

A. Dual Input Single Output Differential Amplifier

Circuit Diagram of Proposed Comparator is shown in figure 3 .This circuits mainly is a derived version the back-to-back latch stage is replaced with back-to-back dual input single output differential amplifier. Differential amplifier has so many advantages over the conventional latch which nothing but an inverter. It has higher immunity to environmental noise. And it rejects common mode noise or in other words it has better CMRR. Another property of differential signaling is the increase in maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Here our main purpose is to eliminating the noise that is present in

the latch stage and for which output is getting fluctuated with clock transition.

B. Operation

During reset phase (clk= 0V), PMOS transistor M4 and M5 turn on and they charge Ni node voltages to VDD. And Hence NMOS transistors M 17 and M 19 turns on and discharges Ni' nodes voltages to GND. Then M14, M15 and PMOS transistors of differential amplifier blocks M12 and M13 turns on, NMOS transistors of differential amplifier block M8, M9 and M6, M7 turns off. The out nodes are charges to VDD. During evaluation phase (clk= VDD), the Ni node capacitances are discharged from VDD to GND in a rate which is proportional to the input voltages.

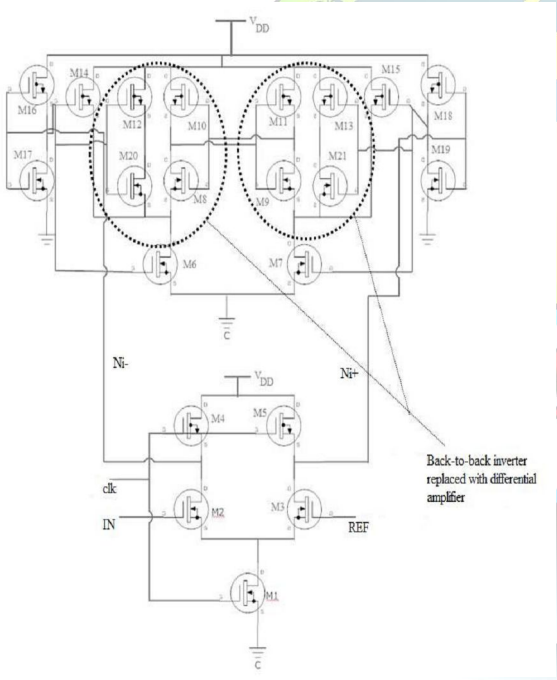

Fig 3 Schematic diagram of dual input single output differential amplifier

At a certain voltage of Ni nodes, the inverter pairs M16/M17 and M18/M19 invert the Ni node signal into a regenerated signal. These regenerated signals turn PMOS transistors M14, M12, M13, and M15 off. And eventually M6, M7, M20, M21 turns on. Hence the back-to-back differential pair again regenerates the Ni' node signals and because of M6 and M7 being on, the output latch stage converts the small voltage difference transmitted from Ni' node into a full scale digital level output.

IV. Conclusion

A new dynamic comparator using positive feedback which shows better noise response, higher speed, lower power dissipation than the conventional dynamic latched comparator has been proposed & targeted for ADC application. The results are simulated in model-sim. In the proposed design, the back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. Output of the latch stage in the proposed design is not affected by noise. The noise present in the input and the clock is completely suppressed by the differential amplifiers present in the output latch stage. The proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature. The transistor count in the proposed comparator is higher to an extent among all the comparators analysed.

.

References

[1]. Nikoozadeh and B. Murmann, "An analysis of latched comparator offset due to load capacitor mismatch," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.

[2]. A. Matsuzawa ,M. Miyahara, P. Daehwa and Y. Asada , "A Low- Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," in Proc. A-SSCC, pp.269-272, Nov. 2008.

[3]. Wicht, D. Schmitt-Landsiedel and T. Nirschl, "Yield and speed optimization of a latch-type voltage sense amplifier", IEEE J. Solid- State Circuits, vol. 39, pp. 1148-1158, July 2004.

[4]. Murmann and Nikoozadeh , "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits .Exp. Briefs, vol. 53, no. 12, pp. 1398-1402, Dec. 2006.

[5]. B. Murmann et al., "Impact of scaling on analog performance and associated modeling needs," IEEE Trans. Electron Devices, vol. 5 no. 9, pp. 2160-2167, Sep. 2006.

[6]. B. Nauta ,D. Schinkel, E. Mensink, E. Kiumperink and E. van Tuij "A Double-Tail Latch-Type Voltage Sense Amplifier with18psSetup+Hold Time," ISSCC Dig. Tech. Papers, pp. 314-315 and 605 Feb. 2007.

[7]. B. S. Leibowits , C. J. Madden ,J. Kim and J. Ren, , "Simulation and analysis of random decision errors in clocked comparators," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 8, pp. 1844– 1857, Aug. 2009.

[8]. Johns and K. Martin, "Analog Integrated Circuit Design," New York,USA: Wiley, 1997.

[9]. David E. Boyce, Harry W. Li, R. Jacob Baker , "CMOS- Circuit Design, Layout, And Simulation", IEEE Press Series on

Microelectronic Systems, IEEE Press, Prentice Hall of India Private Limited, Eastern Economy Edition,2002

[10]. Douglas R. Holberg and Philip E. Allen , "CMOS Analog Circuit Design, 2nd ed., Oxford Indian Edition, 2006.

[11]. Degang Chen ,Jun He, R.L. Geiger and Sanyi Zhan, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.

BIOGRAPHY

Ms.Sankari did her Bachelor Degree in Electronics and Communication engineering and Master Degree in VLSI DESIGN. Now working as a Assistant Professor in M.A.M College of Engineering and Technology, Trichy. She has taught subjects like VLSI Design and Linear and Transmission lines and Waveguides. She has presented Research papers in various conferences.

First Author Mr.S.Belwin Joel did his Bachelor of Engineering degree in Electronics and Communication Engineering and his Master of Engineering Degree in VLSI DESIGN And now working as a Assistant Professor in James College of engineering and technology, Nagercoil. He has taught subjects like VLSI Technology and Linear Integrated Circuits. He has presented many Research papers and Articles in various conferences & seminars.

Second Author Ms.Siraj did her Bachelor Degree in Electronics and Communication engineering and Master Degree in Applied Electronics. Now working as a Assistant Professor in M.A.M College of engineering and Technology, Trichy. She has taught subjects like Low Power VLSI Design, Microprocessor and Microcontroller and Electronic Circuits. She has presented Research papers in various Conferences.