ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. II, Special Issue XVIII,February 2015 in association with
KINGS COLLEGE OF ENGINEERING, PUNAL KULAM, THANJAVUR – 613303
DEPARTMENT OF INFORMATION TECHNOLOGY
NATIONAL CONFERENCE ON RECENT TRENDS IN INFORMATION TECHNOLOGY (NCRIT'15)
13TH MARCH 2015

LINEARITY ANALYSIS OF SPLIT SAR ADC USING Vcm BASED SWITCHING AND SWITCHBACK SWITCHING FOR WIRELESS SENSOR NETWORK

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ABSTRACT: As advanced CMOS technologies enhance the prepared speed of logic circuit significantly. Successive approximation register (SAR) analog-to-digital converter is well-matched with the standard CMOS process with low provides voltage, because it does not need ready amplifiers. A precious alternate is the split capacitive DAC, which has been lately reconsider for average resolution. High speed and medium-to-high resolution usually call for pipeline, two-step, or sub ranging schemes. The basic structure blocks are the track-and-hold, the comparator, and the op-amp. Its key drawback lies in the parasitic capacitors that demolish the desired dual ratio of the capacitive DAC array, thus corrupting the conversion linearity. The competitive power utilization performance of a SAR architecture has been extended with a sub range architecture using a Flash in front of the SAR. The SAR speed boundary doubles by plummeting the accuracy from 9 bit to 5 bit. In previous methods are conventional charge redistribution and Vcm based switching techniques. Some drawback are there in existing methods. To improve the Speed and reduce the power consumption the another method is switch back switching method. In this method to overcome all the drawbacks. The switchback switching method consumes low power compare with the monotonic and Vcm based switching methods during the conversion phase.

Key words: SAR, switchback switching, dynamic comparator

INTRODUCTION : Wireless sensor networks (WSN) contain multiple sensor nodes. In most cases, changing their batteries is impractical or impossible, therefore battery-less devices that collect energy from the environment are essential. A variety of energy harvesting technologies, such as solar power, RF power and

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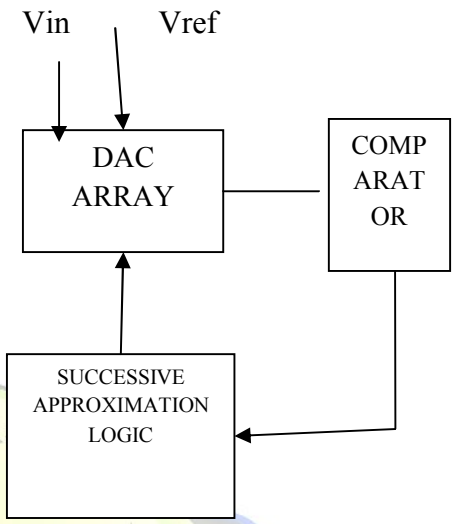
mechanical vibration, can be utilized as power sources to provide a supply voltage of around 0.6 V.1. Therefore, ultra low voltage operation with high power efficiency is desirable for WSN applications. The analog-to-digital converter (ADC) is a primary block for all sensor node. Among dissimilar conversion topologies, the SAR ADC is known for its low power, little area and capability to operate below a low supply voltage. The split capacitor array is more gorgeous than conventional binary-weight capacitor (BWC) array because of smaller input equivalent capacitance and lower power utilization. However, the parasitic capacitance reduces the linearity of the DAC array, which degrades the overall performance of the ADC. Particularly in up to date nanometer technology, small unit capacitors are frequently used fit to speed and power consideration, which causes more non-idealities for the split capacitor array because the freeloading outcome becomes more critical.



Dynamic comparator with offset cancellation:

As is shown in Fig. 3, the comparator is a two stage dynamic comparator which is relatively power well-organized. The first stage is a voltage amplification stage with a discrepancy pair. The latching stage contains an appreciation amplifier to achieve the rail to rail digital output. Earlier than the comparison, the amplification stage output is electric to near VDD. A rising CLK edge stops the pre-charging and starts the amplification in the first stage. Then the familiar voltage of the output of the first stage decreases when it approaches the threshold of the input of the second step, the reaction back-to-back inverters was

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triggered to grant the output. This comparator has no power indulgence when the comparator is not dynamic. As this type of dynamic comparators cannot apply analog feedback, and auto-zeroing is also not needed. For the dynamic comparator, the offset voltage preserve be canceled all the way through adjusting the weight capacitance the current or the threshold voltage of the differential pair. Though, the method of controlling the load capacitance degrades the respond. The present calibration procedure introduces exploits extra one pair of NMOS compensation transistors in corresponding with the degree of difference input pair and a charge pump. But the calibration course of action has to be done regularly from the time when the charged voltage in the damages capacitor cascade down owing to the leakage current. In accumulation, the calibration speed and precision are incomplete by the size of the charging or discharging current sources of allege pump. Therefore adjusting the differential pair's threshold voltage technique is chosen.

Related work:

In [1] *C. C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin et al presents A 0.92 mW 10-bit 50-MS/s SAR ADC in 0.13 μm CMOS process. In this a* predictable successive approximation register (SAR) ADCs, the primary sources of power debauchery are the digital control circuit, comparator and the DAC capacitor selection. The digital power reduces with development of knowledge. However, the control of comparator and capacitor network is imperfect by in excellence and noise issues.

In [2] *K. Chandrashekar and B. Bakkaloglu* et al presents *A 1.8-V 22-mW 10-bit 30MS/s pipelined CMOS ADC for low-power subsampling applications*. The ADC adopts a power well-organized amplifier distribution architecture in which supplementary switches are introduced to reduce the crosstalk between the two op-amp allocation successive stages. A new pattern is used in the first stage of the ADC to stay away from using a enthusiastic sample-and-hold amplifier (SHA) circuit at the input and to avoid the corresponding constraint between the first multiplying

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digital-to-analog converter (MDAC) and flash input indication paths.

In [3] *U.-F. Chio, H.-G. Wei, Z. Yan, S. Sai-Weng, U. Seng-Pan, R. P. Martins, and F. Maloberti* presents *Design and experimental verification of a power effective Flash-SAR subranging ADC* The architectural concept of an most favorable sub ranging ADC, obtained with the tumble of a Flash and a SAR, which is also explored during its realistic design and experimental verification. The answer doubles the best possible speed of operation of the SAR ADCs at the qualified low power cost of a low-resolution Flash. The digital modification method and a capacitor-based DAC make certain no challenging requirements for the Flash.

In [4] *Y. Zhu, C.-H. Chan, U.-F. Chio, S.-W. Sin, U. Seng-Pan, and R. P. Martins* et al presents *A voltage feedback charge compensation technique for split DAC architecture in SAR ADCs*. The charge payment is achieved by using an open loop amplifier that performs voltage feedback to the DAC array via a reimbursement capacitor, which is easy to be implemented with very low power dissipation.

In [5] *B. P. Ginsburg and A. P. Chandrakasan* presents *An energy-efficient charge recycling approach for a SAR converter with capacitive DAC* .The exploit of the supply voltage as the suggestion of the ADC would guide to a signal hang of the converter that is wider than the characteristic signal range; this would shrink the efficient SNR. This drawback is detached with the proposed technique that grants a submissive gain by 2 of the input. A repetition of the LSB, that relaxes the restrictions of noise and make up for, also lowers the power consumption of the comparator.

Proposed System:

Successive Approximation ADC

A successive approximation ADC is a type of analog-to-digital converter that converts a nonstop analog waveform into a disconnected digital illustration via a binary search through all feasible quantization levels before lastly converging upon a digital output for each translation.

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The successive approximation Analog to digital converter circuit normally consists of four chief sub circuits:

A sample and hold circuit to attain the input voltage (V_{in}).

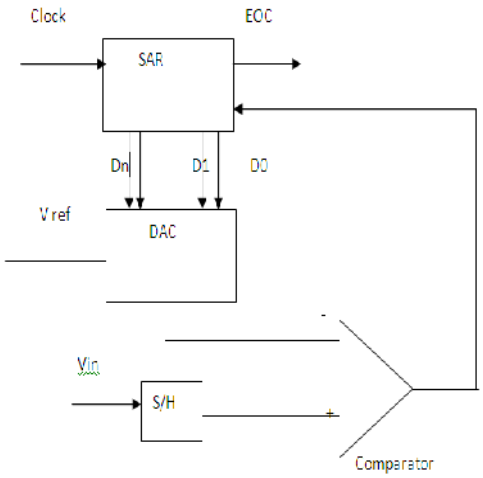
An analog voltage comparator that compares V_{in} to the output of the interior DAC and outputs the consequence of the association to the successive approximation register (SAR).

A successive approximation register sub circuit considered to supply an approximate digital code of V_{in} to the domestic DAC.

An internal reference DAC that, for evaluation with V_{REF}, supplies the comparator with an analog voltage equal to the digital system output of the SAR_{in}.

The successive approximation register is initialized so that the most significant bit (MSB) is equal to a digital 1. This code is fed into the DAC, which then equipment the analog corresponding of this digital code ($V_{ref}/2$) into the comparator path for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit; otherwise, the bit is left a 1. Then the next bit is set to 1 and the same test is done, long-term this binary search until every bit in the SAR has been tested. The ensuing code is the digital estimate of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

SAR Logic Control:



ADC architecture

The SAR structural design mostly uses the binary search algorithm. The SAR ADC consists of smaller amount blocks

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such as one comparator, one DAC (Digital to Analog Converter) and one control logic.

A successive approximation (SAR) ADC using binary weighted split capacitor array DAC. The basic algorithm of binary look for is to exchange analog signal into digital signal/quantized form. The conversion procedure starts after discharging the capacitors. During sampling mode capacitor array is charged by vIN (input voltage). During charge reorganization mode, MSB (Most Significant Bit) set to one and outstanding bits set to zero. The MSB capacitor is charge to Vref (Reference Voltage). If Comparator output is high, bottom plate of MSB capacitor remains connected to Vref. On the other hand, if comparator output is low, the MSB capacitor connects to the ground. The conversion process continue for the next largest MSB same way, and the second largest capacitor charges to Vref while the outstanding LSB (Least Significant Bit) capacitor selection connect to the ground. If the comparator output is high, the second principal MSB capacitor connects to Vref or else it connects to the ground. This process continues awaiting the last adaptation.

ADVANTAGES AND LIMITATIONS

The main advantage of SAR ADC is high-quality ratio of speed to power. The SAR ADC has compressed design compare to flash ADC, which makes SAR ADC economical. The physical restriction of SAR ADC is, it has one comparator during the complete discussion process. If there is any make up for error in the comparator, it will return on the all adaptation bits. The other source is gain error in DAC. However, the static constriction errors do not influence dynamic activities of SAR ADC. Additionally, higher the speed, it is complex to attain the energetic behavior of ADC. One clarification is to use time-interleaved converters.

IMPLEMENTATION RESULTS:

This graph shows that the sample and hold circuit output for the ADC. Cmp denote the

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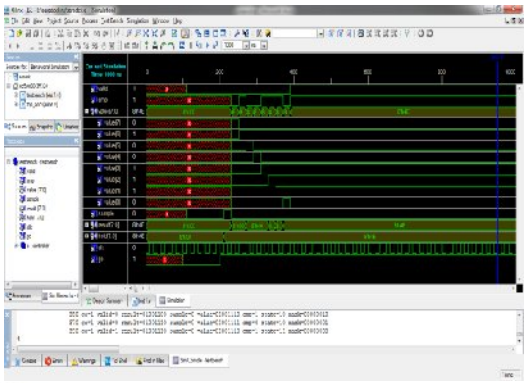
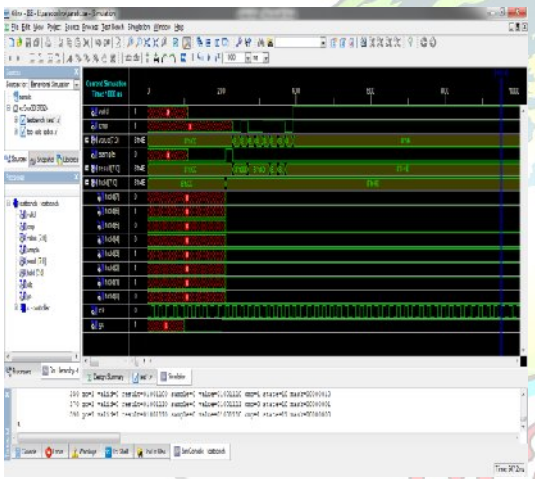
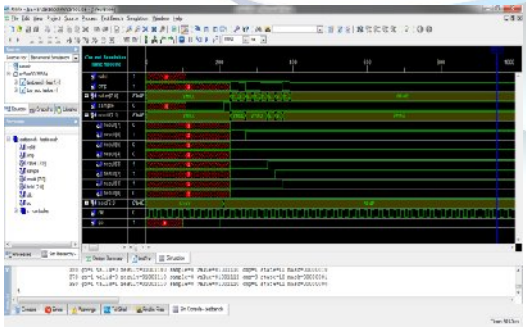
comparator circuit output. The value [7:0] denotes the value of the input signal. Sample denotes the output of the sample circuit. In our proposed system both delay and power of the circuit is reduced due to the efficient switching circuit and non binary conversion algorithm. Speed is high. The value is changed depending upon the state variable.







CONCLUSION:

The INLs of the two switching methods represent the conversion error that combines together all the errors in each bit. The proposed system is also used to improve the Differential Non Linearity and Integral Non Linearity .Considering that in *V*cm-based switching, the transitions are *V*cm related (with capacitors connected to *V*cm), it follows that the INLs of the two switching methods must be different. However, this parasitic nonlinearity effect is irrelevant: the parasitic of the preamplifier input is quite small when compared with the total capacitance of the DAC array. The capacitor matching and parasitic capacitances which directly affect non-linearity parameters of the ADC such as integral non-linearity

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(INL) and differential non-linearity (DNL) are the dominant factors for medium resolutions. The *V*cm-based switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The switch back switching procedure of the monotonic switching procedure only switches a capacitor in every bit cycles, so it reduces the charge in the capacitive DAC network as well as the transitions of the control circuit and switch buffer, it results the low power dissipation. In this technique is used to improve the linearity and increase the speed of operation and reduce usage of power level function.

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